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TRANSMITTAL FORM

Commissioner for Patents

U. S. Department of Commerce

P. O. BOX 1450

Alexandria, VA 22313-1450

Date: May 18th, 2005

Title :	LOW POWER SENSING SCHEME FOR THE SEMICONDUCTOR MEMORY
Inventor :	Chih-Ta Star Sung
Serial No. :	10/724,492

Sir:

Serial No. :	10/724,492
Filed :	12/01/2003
Title :	LOW POWER SENSING SCHEME FOR THE SEMICONDUCTOR MEMORY

A response is enclosed.

Respectfully submitted,

 May, 18th, 2005

Chih-Ta Star Sung

(Applicant/Inventor)



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : SUNG, CHIH-TA STAR Attorney Docket NP-2059
No. :
Serial No. : 10/724,492 Group Art Unit: 2827
Filed : 12/01/2003 Examiner: Michael t. Tran
Title: LOW POWER SENSING SCHEME FOR THE
SEMICONDUCTOR MEMORY

Honorable Commissioner for Patents
U. S. Department of Commerce
P. O. BOX 1450
Alexandria, VA 22313-1450

Dear Sir:

This paper is in response to the Official Action mailed February 24, 2005. Applicants respectfully submit the following amendments and comments in connection with the above-named application.

Amendment

IN THE CLAIMS:

Please amend Claim 1, Claim 8 and Claim 9 as follows:

Claim 1. (Amended)

A semiconductor memory sensing circuit in a memory array,
comprising: